

ABSTRACT

A multiply unit uses four multipliers independently to perform for four parallel multiplications of single-width operands or uses the four multiplier cooperatively with an adder to perform a multiplication of double-width operands. In alternative embodiments, the adder operates in the same clock cycle as the multipliers or in a following clock cycle. Operand selection logic selects pairs of either single-width multiplicands or single-width partial multiplicands depending on for single or double-width multiplies.

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